

WHAT IS CLAIMED IS:

1. 1. A method for protecting integrated circuitry from induced charge damage during device fabrication, the method comprising:
 3. forming an ONO layer on a substrate, the ONO layer having an opening therein;
 5. filling the opening with a thin insulating layer; and
 6. forming a polysilicon layer on the ONO layer and the thin insulating layer.
1. 2. The method of claim 1 wherein filling the opening with a thin insulating layer comprises providing an oxide layer with a thickness of no more than about eighty Angstroms.
1. 3. The method of claim 2 further wherein the thicknesss of the thin oxide layer is less than about 60Å.
1. 4. The method of claim 1 further comprising creating an n-well in the substrate prior to forming the ONO layer, where the opening in the ONO layer is over the n-well.
1. 5. The method of claim 4 further comprising forming an n+well at a junction between the substrate and the n-well.
1. 6. The method of claim 4 further comprising creating a p-well within the n-well, wherein the opening in the ONO layer is over the p-well.
1. 7. The method of claim 6 further comprising forming a p+well adjacent the p-well.
1. 8. The method of claim 1 further comprising isolating the thin oxide layer from the substrate with a PN junction.
1. 9. The method of claim 1 further comprising isolating the thin oxide layer from the substrate by a pair of back-to-back PN junctions.

1 10. The method of claim 9 wherein the PN junctions function as diodes.

- 1 11. A structure for protecting NROM devices from charge induced damage during
- 2 device fabrication, the structure comprising: a substrate;
- 3 an ONO layer disposed on the substrate, the ONO layer having an opening
- 4 therein;
- 5 a thin insulative layer disposed on the substrate within the opening in the
- 6 ONO layer; and
- 7 a polysilicon layer disposed on the ONO layer and on the thin insulative layer
- 8 the polysilicon layer being coupled to circuitry to be protected.
- 1 12. The structure of claim 11 wherein the thin insulative layer comprises a thin
- 2 oxide layer.
- 1 13. The structure of claim 12 wherein the thin oxide layer has a thickness less than
- 2 about 80Å.
- 1 14. The structure of claim 13 wherein the thin oxide layer has a thickness less than
- 2 about 60Å.
- 1 15. The structure of claim 12 further comprising a first PN junction between the
- 2 thin oxide layer and the substrate.
- 1 16. The structure of claim 15 wherein the first PN junction comprises an n-well in
- 2 a p-type substrate.
- 1 17. The structure of claim 16 further comprising a second PN junction.
- 1 18. The structure of claim 17 wherein the second PN junction comprises a p-well
- 2 within the n-well.
- 1 19. The structure of claim 18 further comprising an n+well at a junction between
- 2 the n-well and the substrate.
- 1 20. The structure of claim 19 further comprising a p+well adjacent to the p-well.